2817

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No: 09/596,863
Filed: June 19, 2000
Inventor(s):
Novak, Istvan

Examiner: Bettendorf, J.
Group/Art Unit: 2817
Atty. Dkt. No: 5181-62800

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Erik A. Heter
Printed Name

Signature 2/15/03 Date

Title: BYPASS CAPACITOR METHODS FOR ACHIEVING A DESIRED VALUE OF ELECTRICAL IMPEDANCE BETWEEN PARALLEL PLANAR CONDUCTORS OF AN ELECTRICAL POWER DISTRIBUTION STRUCTURE AND ASSOCIATED ELECTRICAL POWER DISTRIBUTION STRUCTURES

#14/Response
Marsha
2/24/03

RESPONSE TO OFFICE ACTION OF November 15, 2002

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This paper is submitted in response to the Office Action of November 15, 2002, to further highlight why the application is in condition for allowance.

REMARKS

Claims 1-15 and 17-35 are currently pending in the application.

35 U.S.C. § 103 Rejection

Claims 1-15 and 17-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Harada, et al., U.S. Patent 6,198,362, in view of Roy et al., "ESR and

ESL of Ceramic Capacitor Applied to Decoupling Applications" and Novak, "Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination". Applicant respectfully traverses this rejection.

The cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. Harada teaches a printed circuit board. A top layer power supply pattern and a top layer ground pattern are formed. The top layer power supply pattern and the top layer ground pattern are connected to a power supply layer and a ground layer through a plurality of viaholes, respectively. A plurality of capacitors or a plurality of capacitor resistor series circuits are disposed at predetermined intervals between the top layer power supply pattern and the top layer ground pattern.

Roy teaches that power distribution system noise affects computer product timing performance, signal integrity and electromagnetic interference. Between 1 MHz and 1 GHz, the primary means of reducing power distribution noise is with ceramic decoupling capacitors. To achieve a certain target impedance, it is important to characterize the ESR of ceramic decoupling capacitors as they directly determine the number of capacitors required on the board. Another factor which determines the capacitance value of decoupling capacitors is the ESL (inductance) associated with capacitors mounted on a PCB.

Novak teaches that power and ground planes should exhibit low impedance over a wide range of frequencies. Parallel ground and power planes in multilayer printed-circuit boards exhibit multiple resonances which increase the impedance and also the radiation from the edge of the board. Resistive termination along the board edges reduces the resonance peaks.

In contrast, Applicant teaches an electrical power distribution structure and methods to achieve a target electrical impedance therefor. Independent claim 1 recites, in pertinent part:

"wherein the mounted inductance L_m of each of the n capacitors is less than or equal to $(0.2 \cdot n \cdot \mu_0 \cdot h)$, and wherein μ_0 is the permeability of free space, and wherein h is a distance between the planar conductors" (Emphasis added).

Similarly, independent claim 8 recites, in pertinent part:

"determining a required number n of a selected type of discrete electrical capacitor dependent upon an inductance of the electrical power distribution structure L_p and a mounted inductance L_m of a representative one of the selected type of discrete electrical capacitor when electrically coupled between the planar conductors, wherein $n \geq 2$, wherein the mounted inductance L_m is less than or equal to the inductance of the electrical power distribution structure L_p" (Emphasis added).

Independent claim 17 recites a similar combination of features.

Neither Harada, Novak, nor Roy teach or suggest this combination of features. In particular, none of the cited references teaches or suggests selecting capacitors such that their mounted inductance is less than or equal to the inductance $(0.2 \cdot n \cdot \mu_0 \cdot h)$. In the office action, the Examiner states that this is an inherent limitation and further states that the "inherency of the mounted inductance being less than or equal to Lp or $0.2 \cdot n \cdot \mu_0 \cdot h$ is based on the fact that the Harada et al. reference discloses that the undesired wave radiated from the power supply is suppressed, which is the requirement for the value of the mounted inductance (col. 7, lines col. 50-65 and figure 6). That is, the undesired electromagnetic wave would not be suppressed unless the mounted inductance is less than the limit recited in the independent claim." Column 7, lines 50-65 of Harada state:

> "At this point, an undesired electromagnetic wave radiated from the power supply system composed of the power supply layer and the ground layer resonates at around 170 MHz and 480 MHz as denoted by peaks of a dotted curve shown in FIG. 6. In this frequency band, the

resonance characteristic of the power supply system depends on the inductance component of the decoupling circuit. When the inductance component is decreased, the impedance between the power supply layer and the ground layer is decreased. Thus, an undesired electromagnetic wave radiated from the power supply system can be suppressed.

The parasitic inductance of the decoupling circuit can be decreased with the same decoupling circuit connected in parallel thereto. When n decoupling circuits with parasitic inductance L each are connected in parallel, the total inductance can be decreased to L/n. In other words, the parasitic inductance can be decreased by connecting the power supply layer and the ground layer with a plurality of viaholes and capacitors as with the printed circuit board 1 shown in FIG. 1."

Applicant respectfully disagrees with the Examiner's statements that the undesired electromagnetic wave would not be suppressed unless the mounted inductance is less than the limit recited in the independent claims, and further disagrees that the limits recited in the independent claims are inherent. Applicant submits that capacitors used to suppress an undesired electromagnetic wave do not inherently have, nor are required to have, a mounted inductance that is less than or equal to an inductance of $(0.2 \cdot n \cdot \mu_0 \cdot h)$ or a mounted inductance that is less than or equal to an inductance of an electrical power distribution structure L_p. Furthermore, Applicant can find no teaching or suggestion whatsoever in Harada that a mounted inductance of less than or equal to $(0.2 \cdot n \cdot \mu_0 \cdot h)$ for each of the n selected capacitors is required to suppress an undesired electromagnetic wave, or any teaching or suggestion whatsoever that a mounted inductance that is less than or equal to the inductance of the electrical power distribution structure (L_p) for each of the n selected decoupling capacitors is required to suppress an undesired electromagnetic wave. Furthermore, Applicant can find no teaching or suggestion in Harada of any specific relationship between the mounted inductance value for a selected capacitor and the inductance of the electrical power distribution structure. Accordingly, applicant submits that the independent claims are not obvious. Removal of the § 103(a) rejection is respectfully requested.

Allowed Claims:

Claims 31-35 were allowed. Applicant appreciates Examiner's consideration of these claims.

CONCLUSION

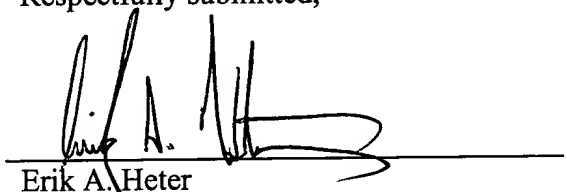
Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 50-1505/5181-62800/BNK.

Also enclosed herewith are the following items:

[X] Return Receipt Postcard

Respectfully submitted,



Erik A. Heter
Reg. No. 50,652
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: 2/3/03